forming a second gate structure including an NWELL using only one mask.

REMARKS

Applicant has reviewed and considered the office action mailed on May 28, 2002 and the references cited therewith.

Support for new claims 45-56 is found on pages 5-8 of the specification.

Claims 45-56 are added; and as a result, claims 1-6, 9, 10, 17, 18, 36, 38 and 45-56 are now pending in the application.

§112 Rejection of the Claims

Claims 1-4, 5-6, 9-10, 17-18 and 36 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant traverses the rejections of claims 1-4, 5-6, 9-10, 17-18 and 36.

The office action states: "The original disclosure does not teach forming a gate structure or dual gate structure using only one mask as recited in present claims 1, 5, 9, 17, and 36." Applicant respectfully disagrees. Applicant submits that the claims are fully enabled by the specification. For example, Figures 4A, 4B and 4C illustrate one embodiment of the invention. A summary description of Figures 4A, 4B and 4C found at page 5 of the specification follows: "Figures 4A-4C illustrate, in a sequence of cross-sectional views, an example embodiment of a dual doped gate structure of the present invention formed using one masking operation after a blanket PWELL is formed through a sacrificial oxide." Even this summary description when read with reference to the drawings clearly discloses to one of ordinary skill in the art how to make a gate structure or dual gate structure using only one mask. Further enablement for this embodiment is provided in the description included on pages 5-8 of the specification. Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 1-4, 5-6, 9-10, 17-18 and 36.

Claims 1-4, 5-6, 9-10, 17-18, 36 and 38 were rejected under 35 U.S.C. § 112, second

paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant traverses the rejections of claims 1-4, 5-6, 9-10, 17-18, 36 and 38.

35 U.S.C. § 112, second paragraph, is directed to claim scope. The office action states: "In claims 1, 5, 9, 17 and 36, it is unclear how a gate or a gate structure is formed using only one mask." However, this statement does not support a 35 U.S.C. § 112, second paragraph claim rejection because it is not directed to claim scope. Thus, the rejection is unsupported and hence improper. Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 1-4, 5-6, 9-10, 17-18, 36 and 38.

Similarly, in rejecting claims 36 and 38 under 35 U.S.C. § 112, second paragraph, the office action addresses issues other than claim scope, so the rejections of claims 36 and 38, under 35 U.S.C. § 112, second paragraph, are improper. Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 36 and 38.

§102 Rejection of the Claims

Claims 1, 3, 5, 6 and 36 were rejected under 35 U.S.C. § 102(b) as being anticipated by Liu (U.S. 6,030,861). Applicant does not admit that Liu is prior art and reserves the right to swear behind Liu as provided for under 37 C.F.R. 1.131. Applicant traverses the rejections.

Liu does not qualify as prior art under 35 U.S.C. § 102(b). Only patents having an effective issue date of more than one year prior to the effective filing date of an application qualify as prior art references under 35 U.S.C. 102(b). Liu's issue date is February 29, 2000. Applicant's effective filing date is February 13, 2001. Since February 29, 2000 is not more than one year prior to February 13, 2001, Liu's issue date is not more than one year prior to the applicant's effective filing date. Thus, Lieu is not prior art under 35 U.S.C. 102(b). Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 1, 3, 5, 6 and 36.

§103 Rejection of the Claims

Claims 9 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu (U.S. 6,030,861). Applicant does not admit that Liu is prior art and reserves the right to swear behind Liu as provided for under 37 C.F.R. 1.131. Applicant traverses the rejections of claims 9 and 10.

Claim 9 recites, "forming a first gate structure including a PWELL having a depth of about 200 nanometers *without using a mask* (emphasis added)." In contrast, Liu, at column 2, lines 1-5 and column 3, lines 1-4, states:

> Referring now to FIG. 1, there is illustrated a cross sectional diagram of a substrate 10 which has formed therein a P-tank 12 and an N-tank 14. These are formed with conventional techniques. Typically this will require a self-aligned *mask* technique wherein an opening is made to expose one of the P-tank 12 or N-tank 14 and impurities of the appropriate conductivity type implanted therein, followed by subsequent masking of the implanted tank and exposing the other non-implanted tank (emphasis added).

Hence, Liu teaches using a mask to form the P-tank, while claim 1 recites "forming a first gate structure including a PWELL . . . *without using a mask* (emphasis added)." Thus, Liu does not teach each of the elements of claim 9, so the office action fails to state a *prima facie* case of obviousness with respect to claim 9. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 9.

The office action on page 5 states: "Liu fails to teach the value of the depth of the P well as recited in present claim 9." Applicant agrees and traverses the 35 U.S.C. § 103 single reference rejection because not all of the recited elements of claim 9 are found Liu. Applicant assumes that the Examiner is taking official notice of the missing element. Applicant respectfully objects to the taking of official notice in a single reference obviousness rejection, and pursuant to M.P.E.P. § 2144.03, applicant traverses the assertion of official notice and requests that the Examiner cite a reference that teaches the missing element. If the Examiner cannot cite a reference that teaches the missing element, applicant respectfully requests that the Examiner provide an affidavit describing how the missing element is present in the prior art. If the examiner cannot cite a reference or provide an affidavit, applicant requests withdrawal of the

rejection and reconsideration and allowance of claim 9.

Claim 10 is dependent on claim 9. For reasons analogous to those provided above and elements in the claim, applicant respectfully submits that the office action fails to state a *prima facie* case of obviousness with respect to claim 10. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 10.

Claims 2, 4, 17, 18 and 38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu (U.S. 6,030,861) in view of Gardner et al. (U.S. 6,051,471). Applicant does not admit that Liu is prior art and reserves the right to swear behind Liu as provided for under 37 C.F.R. 1.131. Applicant does not admit that Gardner et al. is prior art and reserves the right to swear behind Gardner et al. as provided for under 37 C.F.R. 1.131. Applicant traverses the rejections of claims 2, 4, 17, 18 and 38.

In reference to claim 2, the office action on page 4 states: "Liu fails to teach the forming a sacrificial oxide layer on a semiconductor as recited in present claim 2." Applicant agrees and traverses the 35 U.S.C. § 103 single reference rejection because not all of the recited elements of claim 2 are found Liu. Applicant assumes that the Examiner is taking official notice of the missing element. Applicant respectfully objects to the taking of official notice in a single reference obviousness rejection, and pursuant to M.P.E.P. § 2144.03, applicant traverses the assertion of official notice and requests that the Examiner cite a reference that teaches the missing element. If the Examiner cannot cite a reference that teaches the missing element, applicant respectfully requests that the Examiner provide an affidavit describing how the missing element is present in the prior art. If the examiner cannot cite a reference or provide an affidavit, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 2.

In reference to claim 4, the office action on page 4 states: "Liu fails to teach the first gate structure is formed by one blanket implantation as recited in present claim 4." The office action then combines the teachings of Liu and Gardner et al. to establish the missing element. Applicant respectfully submits that the combination is improper. The office action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 U.S.P.Q.2d 1430 (Fed. Cir. 2002). Since

the office action fails to make a statement with regard to a suggestion or motivation to combine the references, the office action fails to provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings. Thus, the office action fails to state a *prima facie* case of obviousness. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 4.

In reference to claim 17, the office action states on page 6, as justification for combining Liu and Gardner, that: "It would have been obvious to one of ordinary skill in the art of making semiconductor devices [to] form the first gate structure by blanket implantation because in doing so the use of masking is avoided." Applicant respectfully submits that the rejection of claim 17 is improper because the justification makes use of impermissible hindsight. A suggestion to combine must come from the prior art and not from applicant's specification or impermissible hindsight. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). Thus, since the combination makes use of impermissible hindsight and is therefore improper, the office action fails to state a *prima facie* case of obviousness. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 17.

In reference to claim 18, the office action asserts that the claim recites only a workable or optimal value for depth developed through routine experimentation and optimization. However, the office action fails to cite a case that establishes this principle. Furthermore, the office action fails to cite a case in the semiconductor arts that follows this principle. In addition, the cases cited in MPEP 2144.05 are directed to concentrations and temperatures, while the claim is directed to a depth in a semiconductor device. Without a proper case citation, applicant respectfully submits that rules established for concentrations and temperatures, especially concentrations and temperatures not related to semiconductors, are not extendable to semiconductor applications. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 18.

In reference to claim 38, the office action fails to provide a teaching or motivation to

combine the references. The office action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 U.S.P.Q.2d 1430 (Fed. Cir. 2002). Paragraph 13 on pages 7 and 8 of the office action fails to identify such objective evidence of record for a finding of a suggestion or motivation to combine the reference teachings. Thus, the office action fails to state a *prima facie* case of obviousness. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 38.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone applicant's attorney at 612-371-2109 to facilitate prosecution of the application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 28th day of August, 2002.

DANNY PADYS
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Danny Padys
Signature

Docket No. 00303.592US1
WD # 459549.wpd

Micron Ref. No. 98-0973

Clean Version of Pending Claims

DUAL DOPED GATES
Applicant: Howard E. Rhodes
Serial No.: 09/782,743

1. A method comprising:
preparing a substrate; and
forming one or more dual gate structures in the substrate using only one mask.

2. The method of claim 1, wherein preparing a substrate comprises:
forming a sacrificial oxide layer on a semiconductor.

3. The method of claim 1, wherein preparing a substrate comprises:
forming a gate oxide layer on a semiconductor; and
forming a polysilicon layer on the gate oxide layer.

4. The method of claim 1, wherein forming one or more dual gate structures in the substrate using only one mask comprises:

forming a first gate structure having a first conductivity in the substrate, the first gate structure being formed using one or more blanket implants; and

forming a second gate structure having a second conductivity in the substrate, the second conductivity having a different value than the first conductivity and the second gate structure being formed using only one masking operation.

5. A method comprising:
preparing a substrate;
forming a first gate structure including a PWELL without using a mask; and
forming a second gate structure including an NWELL using only one mask.

6. The method of claim 5, wherein forming a second gate structure including an NWELL using only one mask comprises:

forming a deep NWELL.

9. A method comprising:

preparing a substrate;

forming a first gate structure including a PWELL having a depth of about 200 nanometers without using a mask; and

forming a second gate structure including an NWELL using only one mask.

10. The method of claim 9, wherein forming a second gate structure including an NWELL using only one mask comprises:

forming a deep NWELL.

17. A method comprising:

preparing a substrate;

forming a first gate structure including only blanket implants; and

forming a second gate structure including an NWELL using only one mask.

18. The method of claim 17, wherein forming a second gate structure including an NWELL using only one mask comprises:

forming an NWELL having a depth of about 200 nanometers.

36. A method of forming one or more dual gate structures, the method comprising:

forming one or more gate structures including a PWELL without a mask;

masking one or more NWELL regions; and

forming one or more gate structures including an NWELL in at least one of the one or more NWELL regions.

38. A method of forming one or more dual gate structures, the method comprising:

forming one or more gate structures including a PWELL using blanket implants;

masking one or more NWELL regions; and

forming one or more gate structures including an NWELL in at least one of the one or more NWELL regions.

45. (New) The method of claim 1, preparing the substrate comprises forming a PWELL in an *n*-type substrate.

46. (New) The method of claim 1, wherein forming one or more dual gate structures in the substrate using only one mask comprises forming one or more complementary metal-oxide semiconductor dual gate structures in the substrate using only one mask.

47. (New) The method of claim 2, wherein forming the sacrificial oxide layer on the semiconductor comprises growing a sacrificial oxide layer to a depth of a few microns.

48. (New) The method of claim 3, wherein forming the gate oxide layer on the semiconductor comprises forming the gate oxide layer having a thickness of between about five nanometers and about ten nanometers.

49. (New) The method of claim 5, wherein preparing the substrate comprises forming a PWELL in an *n*-type substrate.

50. (New) The method of claim 5, wherein forming the first gate structure including the PWELL without using the mask comprises forming the PWELL by a blanket implant of boron ions at about 430 keV.

51. (New) The method of claim 5, wherein forming the first gate structure including the PWELL without using the masking comprises forming the PWELL having a depth of about 200 nanometers.

52. (New) The method of claim 5, wherein forming the first gate structure including the PWELL without using the masking comprises forming the PWELL having a blanket implant of boron ions at about 430 keV and a depth of about 200 nanometers.

53. (New) The method of claim 49, wherein forming the first gate structure including the PWELL without using the mask comprises forming the PWELL by a blanket implant of boron ions at about 430 keV.

54. (New) The method of claim 49, wherein forming the first gate structure including the PWELL without using the masking comprises forming the PWELL having a depth of about 200 nanometers.

55. (New) The method of claim 9, wherein preparing the substrate comprises forming a PWELL in an *n*-type substrate.

56. (New) A method comprising:

preparing an *n*-type substrate;

forming a first gate structure including only blanket implants; and

forming a second gate structure including an NWELL using only one mask.